THE DEVELOPMENT OF AN LED DISPLAY SYSTEM

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Abstract

A design for an ARM and FPGA-based LED display control system is put forth. This system uses the ARM chip S3C2240 as the control core and is based on the RGB three-color LED display's module structure characteristics as well as the dynamic scanning display of the LED display made possible by FPGA technology. It achieved communication through Ethernet and PC, completed data storage and update, display refresh, animation, cycle display, and supported text and picture display on a full-color LED screen that is divided into 256 grayscales. The system also enables remote data transmission.

Paper Identification

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Introduction

LED display technology is quickly becoming the most competitive display medium of the next generation because it combines computer technology, microelectronic technology, and information processing into a single, cohesive whole. These advantages include the ability to display a wide range of colours, a high level of dynamic range, high brightness, a long service life, stable and reliable operation, and more. LED display has found many uses in the modern world, including in banking, securities trading, highway signs, airports, and advertisements. Using an FPGA as the central component of the control system for an LED display, for instance, makes the system more difficult to implement from a business standpoint. Additionally, the price is substantially more than average because a high-performance FPGA processor is required. Using a 32-bit processing unit as the backbone of a control system for an LED display is not flexible enough, as it will necessitate major changes if the screen size of the display is ever modified.

In this study, we introduce an embedded-based control technique for LED colour displays, a novel form of project. the basic function and technical index of LED synchronous display system are coupled with the existing issues in LED asynchronous display system to propose a technical strategy to overcome the key problems. Using the ARM+FPGA technology, this paper considers the ARM system to be a video source, adopts an ARM9 chip as the main control unit and an FPGA chip as the scanning control unit, and is able to effectively simplify the circuit structure while also

increasing the reliability and flexibility of the entire control system.

2. Design Principles and the System's Construction

2.1 Mechanisms of Action of a Colored LED Screen

Full-color LED display screens are analogous to colour televisions in that they use the same colour synthesis method. It chooses a colour palette of red, green, and blue, with each pixel consisting of an LED constituting one of those three hues, and by adjusting the intensity of the LEDs, it can synthesise a wide range of colours. LED colour screens typically have an area greater than 1m2, and they are frequently used in remote viewing situations; as a result, the three types of LED colours that make up each group of pixels still share the same visual space [3] and, when they emit light at the same time, can blend to form a new colour. Therefore, three-color LEDs with varying intensities can create a wide range of colours and hues.

The pixels on an LED electronic display panel are all separate from one another. Because LED light is made up of discrete pixels, its control and driving must occur in digital mode [4]. These pixels' emission states are synchronised with the controller and independently driven. For a video to be displayed in full colour, each pixel's red, green, and blue luminance levels must be adjusted independently while still being completed within the allotted scanning time. Due to the large number of individual pixels that make up a large screen, the system must be able to handle massive amounts of data. While it would be ideal to have a conventional D/A for every pixel point, this is just not feasible, thus we need to find ways to maximise performance while drastically simplifying the system.

Each pixel's bright/dark duty ratio can affect how bright or dark that pixel appears to the human eye. That is to say, we can adjust the light level by adjusting the bright/dark duty ratio of the pixels. The phrase D/T conversion" refers to converting the pixel brightness indicated by the data into the pixel luminescence time used by the LED electronic display panel.

Determine the number of seconds between screen updates as Ts, then use N bits to adjust the brightness of any given pixel.

Specifically: $D = \sum_{i=0}^{n-1} b_i 2^i$ The luminance/darkness ratio of a pixel is given by $T_{0N}/T_S = D / 2\ n = \Sigma_{i=0}^{n-1} b_i\ 2^i / 2^n$, where T_{0N} is the luminescence time corresponding to the value D and I is the pixel index. Because when T_S is short enough, the visual effect of T_{0N} the sum of several time segments is the same with a total length of the same continuousT_{0N}, this expression can be used to realise the prefabricated subtraction counter; however, equipping each pixel with a counter makes the display circuit extremely complex.

Therefore, in general, given N bits of binary data $D = \sum_{i=0}^{n-1} b_i 2^i$, T_S is divided into n segments, and the proper temporal partition function f I is chosen, with the section I specified as follows: $i : T_i = T_S\ f\ (i)$, *(where 0 <f (i)< 1 , I= 0,1,2,..., n -1).* D's location n (b_i) controls the amount of light/darkness emitted by each pixel thanks to the circuit's implementation of this control mechanism.

$$T_{ON} = \Sigma_{i=0}^{n-1} T_i b_i = T_S \Sigma_{i=0}^{n-1} f\ (i) bi$$

Now $$d = T_{ON}/T_S == T_S \Sigma_{i=0}^{n-1} T_i b_i / T_S = \Sigma_{i=0}^{n-1} f\ (i) b_i$$

This value represents the pixel's duty cycle, or the perc entage of time it is either light or dark.Since the foregoi ng demonstrates that the function f I is common to all p ixels, we need only utilise f I to synchronise the D/T co nversion of each pixel in the complete display to ensur e that no two pixels are out of sync with one another.

2.2 Developing a Control System for an LED Display

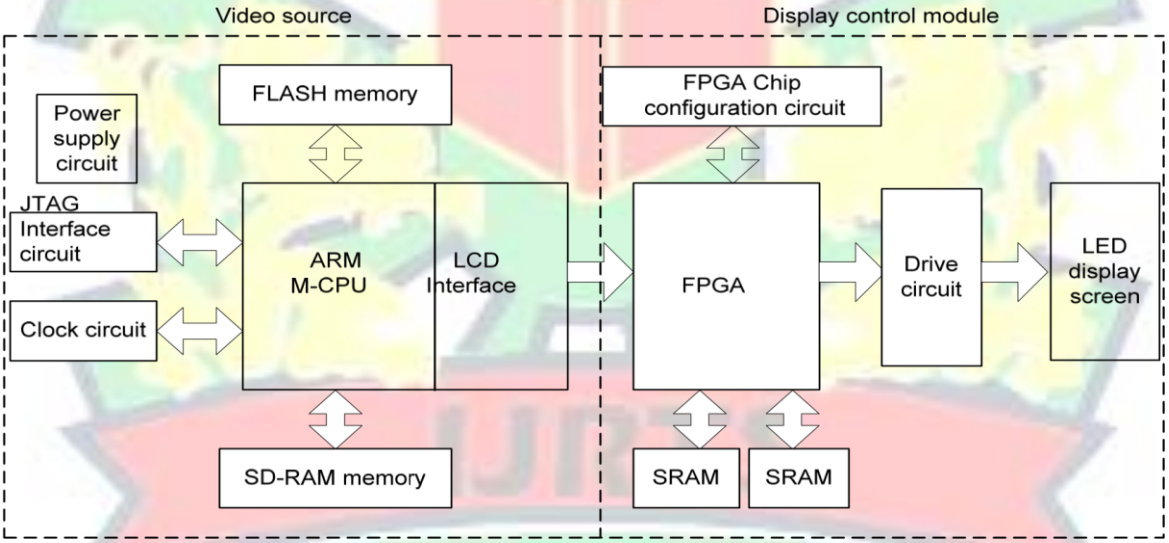
The following are some of the goals that were taken into consideration throughout the system's design:

1. The ARM system can be used as a data source instead of the host computer, allowing the LED display system to be used in an off-line display mode.
2. The display's specifications are 128 columns by 256.
3. Red, green, and blue are the primary colours displayed on an LED screen, and the display can refresh at a rate of 70 times per second.
4. It is capable of grayscale display with 256 grey levels, depending on the desired effect of the displayed images.
5. It can receive the information and settings displayed on the PC via the serial port.

memory and sends the information to a scanning control module that uses FPGA technology [5], which in turn sends the processed image data to the LED screen. Block diagram 1 shows the control system block diagram for an LED display.

The software development and simulation phase focuses primarily on the creation of an ARM embedded software and an FPGA control module.

1. To meet the specifications of the LED display, the design incorporates an embedded system to supply consistent and dependable video. As the video source's nerve centre, the S3C2410 chip was used. Because of its open-source nature, reliability, and robust security, embedded Linux was selected as the software's operating system.



Block diagram 1 of ARM and FPGA-based LED display control system

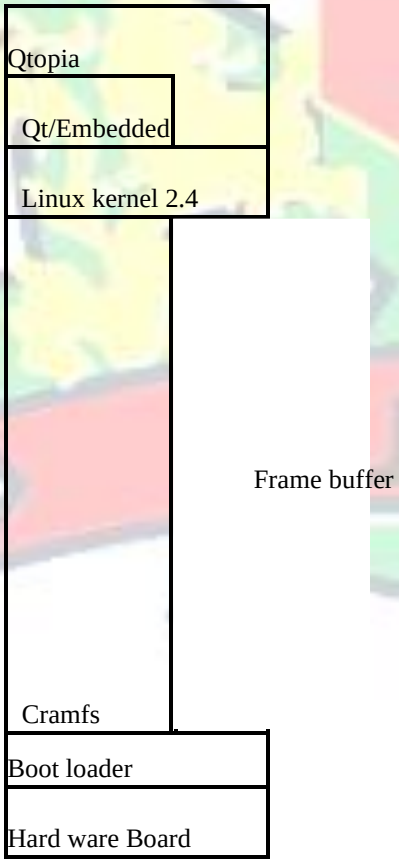
The system picks a 32-bit embedded RISC CPU based on an ARM core and SDRAM as the brains, and a 32-bit FPAG and double RAM as the scanning control module, all in service of realising the aforementioned target function. FLASH is used for storage, and data is transferred through Ethernet. The PC sends the image data to the Ethernet interface module, which performs an examination of the protocol before sending the data on to the control core S3C2410. Finally, the control core S3C2410 stores the data in the NAND FLASH module. When displaying, S3C2410 reads FLASH

Since many embedded systems have already benefited from LCD driver and Qtopia transplantation, it's safe to say that the embedded OS transplantation scheme is well established. Therefore, we'll just gloss over this section.

The boot loader, device drivers, embedded Linux Kernel, file system, and graphical user interface system are the core components of

the S3C2410's software. Figure 2 depicts the platform structure of system software.

2. The ARM system feeds display data and control information to the software element of the FPGA control unit. The data signal and the control signal are then supplied to the LED display screen driving circuit after the display data has been processed and reconstructed, and its meaning has been explained in terms of the weights assigned to various shades of grey in the underlying information. The display control module for LED screens consists of the ARM interface buffer module, the SRAM read/write control module, and the grey scale scanning control module.



System software architecture, as seen in Figure 2.

3. Planned System Hardware Design

3.1 Selection of Processor

The S3C2410 is a processor built on the ARM920T core. S3C2410 features were taken into consideration. S3C2410 processor's working frequency can significantly boost system operation speed, the frequency can make the processor run easily on Windows CE, Linux operating system, and so on, and cope with more complex information, drastically cutting down on software development time; In order to simplify the extension portion of the peripheral circuits and reduce the complexity of the system, the S3C2240 is chosen as the CPU of the system [13]. The S3C2240 has powerful internal interrupts and TCP/IP, both of which can be polling called. There are as many as 117 generic Programmable Multifunction I/O ports, all of which can be connected conveniently with the Ethernet controller RTL8019AS.

3.2 Selection of Memory

This design uses the SDRAM of memory with the highest literacy rate in the embedded application to run as the space of data processing and display, in fact, the chip named K4S561632D is manufactured by SAMSUNG, and it is a synchronous DRAM of 4M16bit4bank, whose size is 32 MB, to meet the needs of large capacity and high speed data processing and to make use of the SDRAM controller interface provided by ARM microprocessor memory interface [10]. Two K4S561632D modules are used to build a 32-MB SDRAM memory system in tandem; one module handles the high 16-bit data, while the second handles the low 16-bit data, giving a 32-bit data bus and 64MB of total storage. Specifically, two portions of K4S561632D's CS ends were linked to the chip select signals of S3C2410's bank6 to create a mapped address space. Figure 3 displays S3C2410's connection to a single SDRAM.

3.3 Circuit design for Ethernet interface

Using an Ethernet circuit module efficiently addresses the issue of far-flung data transfer [6]. The system utilises RealTek's RTL8019AS full duplex Ethernet

controller, which can be easily installed thanks to its plug-and-play capabilities. In addition to the S3C2410's Ethernet expansion capabilities, this chip supports IEEE 802.3, has a full-duplex transceiver with speeds up to 10Mb/s, includes 16KB of on-board SRAM for use as a send/receive buffer, works with an 8/16 data bus, 8 interrupt request lines, and 16 I/O base address selections, and can automatically determine whether a connection is 10Base5 or 10Base2 or 10BaseT. The RTL8019AS and S3C2410 are in jumper mode, there is no EEPROM or ISA bus, all of the pins are connected with high level (JP), the BS[4..0] pins are grounded (only BROM is used), the IOS[2..0] pins are grounded (the base address of the internal registers is 300H), and the interrupt request pin (IRQ2/9) is grounded (the BNC interface uses twisted-pair or coaxial.

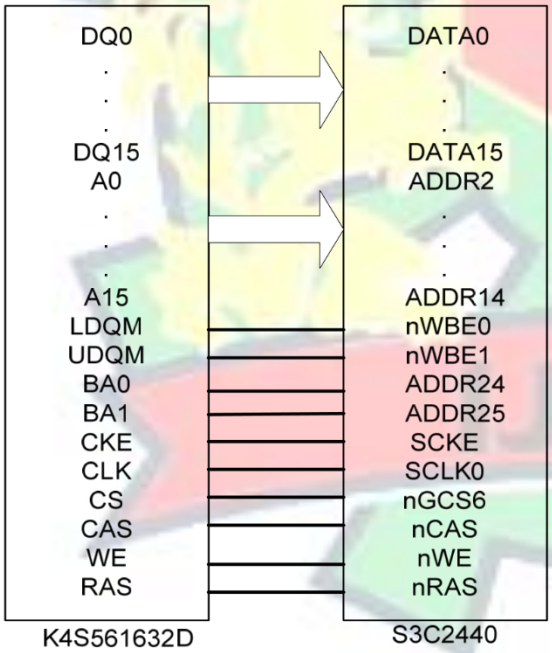


Figure 3: Interface Circuits of control of the core and SD-RAM

3.4 Memory Module Layout Design

To allow for the asynchronous display of the picture source, the memory module of the screen control system must store binary executable code as well as significant volumes of text and image data. This system has decided to use FLASH memory in order to ensure that data such as images and text are safe even if the power goes out, and also because it can provide more storage space than was previously available. The NAND Flash's many benefits—including higher capacity and lower cost than NOR Flash—make it a popular choice for new projects, and S3C2410 is happy to help get them off the ground. This concept combines NAND Flash and SDRAM to provide excellent cost performance [7]. NAND FLASH memory K9F1208 from Samsung Corp is used in the system's memory module due to its enormous storage capacity and great dependability. The K9F1208 is 512 MB (64 M 8-bit) of NAND Flash memory made by Samsung. By using the chip's multiplex 8-bit I/O interface IO[0-7] to read and write the address, data, and control word, it is possible to increase storage capacity without altering the hardware design. Addressing the on-chip control register yields the matching command word that performs the necessary chip-specific operations including reading, writing, and erasing. Next, we'll look at how different state signals typically function: When the write signal WE and the chip selection signal CE are active, the address operation is carried out by enabling ALE effective to latch the address data; when the write sign WE and the chip selection signal CE are active, the data operation is carried out by latching in the rising edge of signals; when the write signal WE and the chip selection signal CE are active, the command word operation is carried out by enabling CLE to latch. S3C2410 and NAND FLASH interface circuit is depicted in Figure 4.

3.5 Planning the Scanner's Control Unit

In order to prevent data loss during scanning, a processing circuit of cache of tell data must be present in an LED display's control system [8]. This is because the display of an LED screen is carried out in contact to tell, and since the scanning of an image's tell is completed in real time in order to accept new data for updating the screen.

The hardware incorporates a field-programmable gate array (FPGA) and dual random-access memory. Read and write operations of double RAM, dubbed table tennis operations, are completed as part of the RGB data buffer implemented by the S3C2410. These activities are controlled by a synchronisation signal. Data processing speed is increased by FPGA, and picture tell scanning and fresh data can be accepted simultaneously thanks to the so-called table tennis operation.

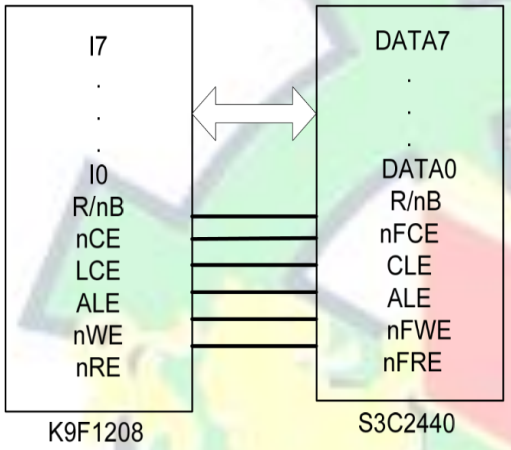


Figure 4. Interface circuits of S3C2410 and NAND FLASH

The module's FPAG is the Altera Cyclone EP1C6Q240C8, a low-cost FPGA with 185 I/O pins, a voltage of 3.3V, a core voltage of 1.5V, and a high working frequency of 200MHz; the FPAG uses 0.13 M technology, SRAM technology made from copper, and has a density of 5980 logical units; it has 20 RAM blocks (M4K modules) with a size. In addition, the on-board RAM block supports shift register and ROM mode, and its clock frequency can be adjusted independently of the input clock's thanks to the clock synthesis function provided by the two on-board phase-locked loop circuits. The output of a single phase-locked loop can be at one of three possible frequencies. EP1C6Q240C8 has the real-time and high-frequency requirements of the design satisfied with its easy operation, high precision, and powerful driving ability.

The required capacity for each frame of a picture on the system's LED display screen is 192Kb, while the resolution of the screen itself is 128x64. Due to the 128K32bit capacity of the IDT71V3577 type of SRAM, the system requires 2 pieces of IDT71V3577 to store a single frame of images. As a result, the system employs a total of 4 IDT71V3577, each of which serves as the system's double RAM and stores information for the display.

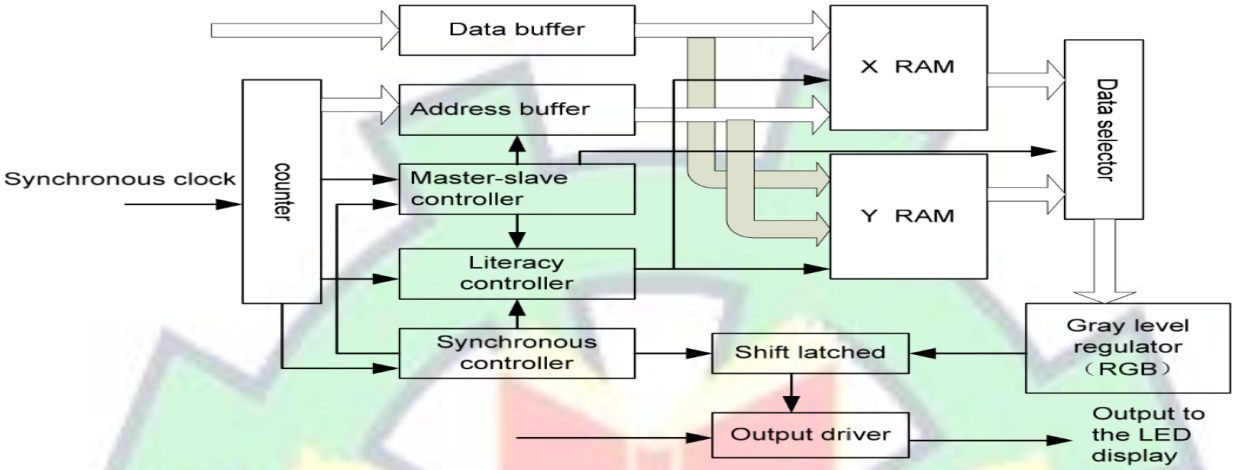
Figure 5 depicts the layout of the scanning and regulating logic circuit [11]. The display memory's writing address and the memory's reading address are generated by the address controller, but it's up to the read-write controller to decide whether to write the data and connect the address with the memory or to read the data and connect the address with the memory. The mode of control circuit design is grey scale display mode to accommodate the screen's image display requirements. Grayscale decoding is followed by a conversion from 4-bit parallel data to 16-bit serial data, the latter of which is suitable for use in an LED screen's display.

The data input rate is 2 Mbit/s, and the data read out rate is 32 Mbit/s, all thanks to the table tennis action of the X, Y two groups of memory, which happens when it receives a frame of parallel data and sends the decoded 16 bit serial data streams to the LED panel. Sending serial data streams at a rate of 32Mbit/s directly to the screen would result in a transmission speed that is too great to manage the data [8]. The 128 by 64 pixel display area of the machine uses an 8 line scanning technique. An 864 grid of scanning units is used to create the scanned area. It is possible to slow down the flow of data with simultaneous scanning of all 16 units. So that it may be scanned and shown, data is written to memory in the proper order, with the grey level decoded into a serial data stream of red, green, and blue at a rate of 32Mbit/s. Display circuits can take use of the 32/16=2 (M bit/s) serial data flow that is achieved after processing [9]. Memory addresses will

no longer work after the time sequence has been written there. The operators controlled by the read/write controller and the address controller sequentially read out data. Furthermore, the synchronous controller produces the clock, latch, and xline scan signals.

4. Conclusion

The aforesaid hardware structure and simulation system architecture allows for an organic integration of PC and embedded control. It also successfully communicates with the Lower PC and displays data on the LED screen.



Scanning circuits' fundamental block diagram 5

In the following simulation waveform diagram of read/write SRAM controll, the signals labelled add write [16:0] and add read [16:0] represent the read/write address of the memory unit to be operated; cs1 and cs2 represent the chip select signals of SRAM1 and SRAM2, respectively; oe1 and oe2 represent their read control signals; and we1 and we2 represent their write control signals.

The built-in control unit allows for effective management of the LED display by allowing for data input and storage, data transformation for display modes, and image output.

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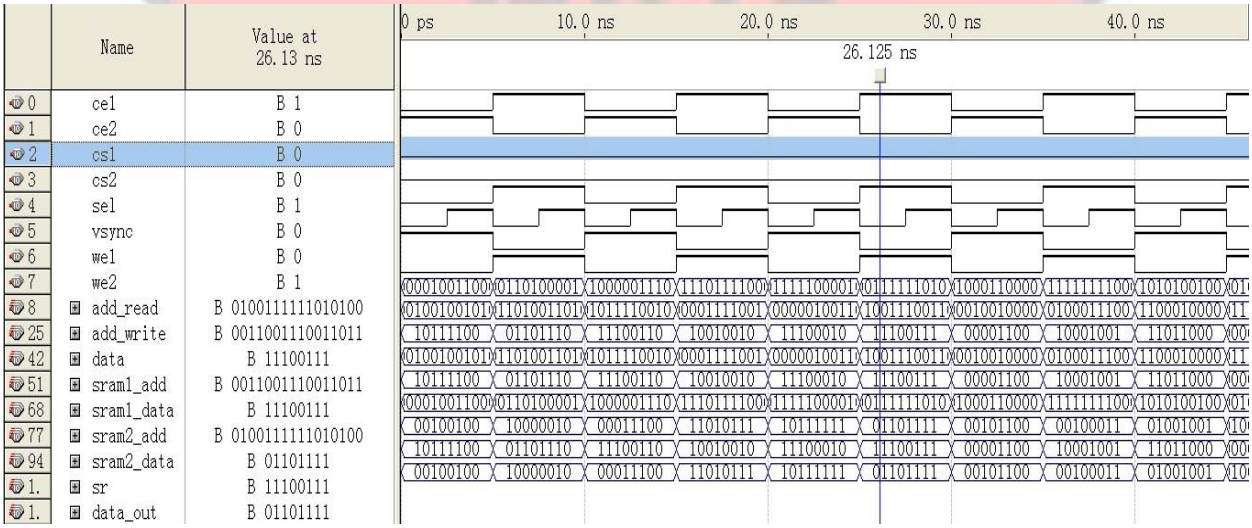

Figure 6: Read/write SRAM command waveform diagram from simulation.

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